GC3021A

3.3V MIXER AND CARRIER REMOVAL CHIP

DATASHEET

October 2002

This datasheet contains information which may be changed at any time without notice.

REVISION HISTORY

This datasheet is revised from the GC3021 datasheet to reflect the changes in the GC3021A replacement.

Revision	Date	Description
1.0	9 Sept2002	First GC3021A datasheet. Major changes in specifications to reflect 3.3volt operation.

0.1 GC3021A TO GC3021 COMPARISON

The GC3021A is designed to be a functional and footprint compatible replacement for the GC3021 chip. The timing specifications for the GC3021A meet and exceed the timing specifications for the GC3021. Electrically the GC3021A is a 3.3 volt only part, making it incompatible with the GC3021's 5 volt mode. The GC3021A does not support the PECL high speed interface from the GC3021. Except for this change, the GC3021A is fully compatible with the GC3021's 3.3 volt mode, but at a lower power consumption. See Section 5 for timing and electrical specifications. NOTE: The GC3021A inputs are NOT 5 volt tolerant; chip damage may occur if the input voltages exceed Vcc + 0.5V (3.8 volts). Designs using the GC3021 at 5 volts will need to add a 3.3 volt supply and voltage level translators to use the GC3021A.

The function of the GC3021A has been slightly enhanced, but any enhancements are "backward" compatible with the GC3021 with the exception of the power down control. In the GC3021A the user must set bit 15 of control register 1. Highlights of the enhancements follow.

0.1.1 Clock Loss Detect and Power Down Modes

The GC3021 chip used a slow internal clock to power down the chip or to put it into a low power mode if the clock is stopped. The slow clock has been removed in the GC3021A and replaced with a mode that will put the chip in a fully static mode if the clock has stopped. The fully static mode powers down the chip and reduces the power consumption down to a few microwatts until the clock resumes. The user can also force the power down state if desired. Two control bits (address 13 bits 6 and 7) are used to control the clock loss detect and power down modes. One control bit turns off the clock loss detect circuit, the other forces the power down mode. Both bits are cleared at power up to keep GC3021 compatibility. THE USER MUST SET POWER DOWN TO A "2" TO OPERATE THE CHIP.

See Section 2.9 for details.

0.1.2 Control Interface

The control interface has been enhanced to use either the R/$\overline{W}$ and $\overline{CS}$ strobes of the original GC3021, or to use the $\overline{RE}$, $\overline{WE}$ and $\overline{CE}$ strobes used by most memory interfaces. If the $\overline{RE}$ pin is grounded, then the interface behaves in the R/$\overline{W}$ and $\overline{CS}$ mode, where the $\overline{WE}$ pin becomes the R/$\overline{W}$ pin and the $\overline{CE}$ pin becomes the $\overline{CS}$ pin. The $\overline{RE}$ pin on the GC3021A chip is a ground pin (pin 58) on the GC3021 chip, so that a GC3021A chip soldered into a GC3021 socket will automatically operate in the GC3021 R/$\overline{W}$ and $\overline{CS}$ mode.

See Section 2.1 for details.

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GC3021A DATASHEET

1.0 KEY FEATURES

CARRIER REMOVAL MODE

- 100 Million Complex Samples per second (CSPS) input data
- 12 bit input and output data
- 12 bit by 12 bit complex multiplier
- 4K bit phase error lookup RAM
- Phase error feedback loop for carrier and phase offset removal
- 32 bit numerically controlled oscillator (NCO)
- Snapshot memory for adaptive filtering

MIXER MODE

- 200 MSPS real input data (even/odd data at 100MSPS)
- 100 MSPS complex input data (TTL level inputs)
- 12 bit inputs and outputs
- 32 bit NCO phase control
- NCO generates 12 bit sines and cosines

OVERALL

- Microprocessor interface for control, output, and diagnostics
- Built in diagnostics
- 500 mW power at 100 MHz, 3.3 volts
- 160 pin plastic quad flat pack package

1.1 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

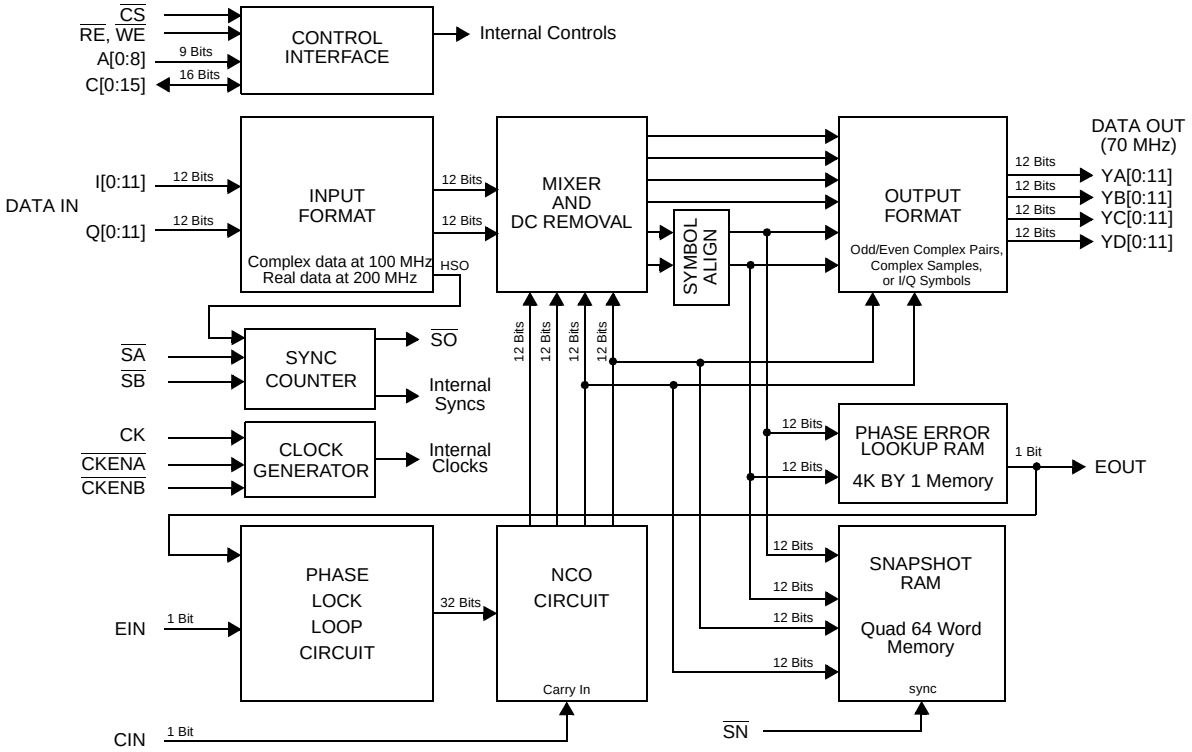


Figure 1. GC3021A BLOCK DIAGRAM

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2.0 FUNCTIONAL DESCRIPTION

Fabricated in 0.5 micron CMOS technology, the GC3021A chip is designed to mix input data with an internally generated sine/cosine sequence. The chip can be used as a signal mixer, or if the phase error lookup and phase lock loop (PLL) circuitry is enabled, as a carrier removal circuit for signal demodulation. The mixer accepts complex data at rates up to 100 MHz , or real samples at rates up to 200 MHz in the real input mode . The chip mixes the input with a complex sinusoid, and outputs the results at a 100 MHz rate.

The input data in the real mode is assumed to be even/odd sample pairs. The 200 MHz input data is split into even and odd samples streams, each at a rate of 100 million samples per second. The even and odd time sample data streams are mixed with sines and cosines which have also been split into even and odd time streams. The complex results are then output as two complex pairs at 100 MHz, one for the even time samples and one for the odd time samples.

The frequency of the sine/cosine sequence is specified as a 32 bit phase word which drives a phase accumulator. A carry input to the phase accumulator allows the user to extend the tuning resolution with an external accumulator.

The GC3021A chip's carrier removal mode allows the chip to be used as part of a QPSK/QAM demodulator using decision error feed back to achieve carrier lock. A phase error feedback circuit uses the upper 7 bits of the I and Q mixer outputs to lookup a one bit phase error term. The phase error lookup is performed by mapping the I/Q pair into a single quadrant so that the lookup table address is only 12 bits (6 bits of I and 6 bits of Q). The 4096 bit lookup table is programmed by the user to output the sign of the phase error for each possible I/Q pair. This phase error feeds a phase-lock-loop (PLL) circuit which adjusts the sinusoid frequency to drive the average phase error to zero.

A snapshot RAM is included to store blocks of I/Q symbol outputs and the sine/cosine pairs used to generate them. This information is used by an external DSP chip or microprocessor to lookup the symbol error, to rotate the error by the sine/cosine phase, and then update equalizer coefficients.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of a 16 bit data I/O port, a 9 bit address port, a read enable, a write enable, and a chip enable strobe. The control registers, coefficient registers, phase error RAM and snapshot memory are mapped into the 512 word address space of the control port.

A detailed description of the major circuits within the chip follows.

2.1 CONTROL INTERFACE

The control interface allows an external processor to configure the chip, to capture and read samples from the chip and to perform diagnostics.

The chip is configured by writing control information into control registers within the chip. The registers are written to or read from using the **C[0:15]**, **A[0:8]**, $\overline{\textbf{RE}}$, $\overline{\textbf{WE}}$, and $\overline{\textbf{CE}}$ pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer,

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or DSP chip) can write into a register by setting **A[0:8]** to the desired register address, setting the **$\overline{CE}$** pin low, setting **C[0:15]** to the desired value and then pulsing **$\overline{WE}$** low. **$\overline{RE}$** must remain high.

To read from a control register the processor must set **A[0:8]** to the desired address, set **$\overline{CE}$** low, and then set **$\overline{RE}$** low. The chip will then drive **C[0:15]** with the contents of the selected register. After the processor has read the value from **C[0:15]** it should set **$\overline{RE}$** and **$\overline{CE}$** high. The **C[0:15]** pins are turned off (high impedance) whenever **$\overline{CE}$** is high or **$\overline{WE}$** is low. The chip will only drive these pins when both **$\overline{CE}$** and **$\overline{RE}$** are low and **$\overline{WE}$** is high.

If **$\overline{RE}$** is held low, then the interface will behave in the GC3021 mode, where **$\overline{CE}$** is **$\overline{CS}$**, and **$\overline{WE}$** is **R/$\overline{W}$**.

The chip's control address space is divided into fourteen control registers, a test port, four DC offset registers, 256 phase error memory words, and 256 snapshot memory words. The 14 control registers are MODE_REG, SYNC_REG0, SYNC_REG1, DELAY_REG, COUNTER_REG, PLL_REG, FREQ_REG0, FREQ_REG1, OUTPUT_REGA, OUTPUT_REGB, OUTPUT_REGC, OUTPUT_REGD, SNAP_REG, and PHASE_REG. The control registers are mapped to addresses 0 to 13. See Section 4.0 for details about the contents of these registers.

Address 14 is used to generate a one-shot pulse. This pulse, $\overline{OS}$, which is one clock cycle wide, can be output from the chip on the $\overline{SO}$ pin or used to synchronize internal circuits. Address 15 is a read only port used to monitor the power-down and keepalive clock functions for test. Addresses 16 through 19 are the DC offset registers DC_I_IN, DC_Q_IN, DC_I_OUT, DC_Q_OUT.

Addresses 20 through 255 are unused.

Addresses 256 through 511 are shared between the phase error memory and the snapshot memory. Reading from these addresses accesses the contents of the snapshot memory. Writing to these addresses loads the phase error lookup memory.

2.2 SYNC COUNTER

The sync counter circuit is used to generate sync pulses for the chip. The circuit accepts two sync inputs ($\overline{SA}$ and $\overline{SB}$) and generates internal syncs and a sync out ($\overline{SO}$) pulse. The circuit contains a 20 bit counter which can be set to count in cycles of 16*(COUNT+1) clocks, where COUNT ranges from 0 to 2^{16}-1. The counter's terminal count ($\overline{TC}$) can be used as a synchronization pulse. The lower 12 bits from the counter are used as input data during diagnostics.

The circuit can generate a one-shot pulse (OS) which can be used as a synchronization pulse.

The input syncs $\overline{SA}$ and $\overline{SB}$ can be delayed by up to 258 clock cycles. The delayed syncs ($\overline{DSA}$ and $\overline{DSB}$) can be used to adjust the sync timing to meet system requirements.

The internal syncs are used to synchronize the counter, the symbol align circuit, the snapshot memory, the phase lock loop circuit and NCO circuit. Each circuit can be independently synchronized to $\overline{SA}$, $\overline{SB}$, $\overline{DSA}$, $\overline{DSB}$, $\overline{TC}$, $\overline{OS}$, or left to free run. The sync output can also be chosen from these syncs.

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2.3 CLOCK GENERATOR

The clock generator generates the internal clocks from the clock input (CK). Two clock enable inputs ($\overline{\text{CKENA}}$ and $\overline{\text{CKENB}}$) are used to enable or disable the clock. Both enables must be low for internal clocks to be generated. The enables are clocked into the chip and are used to enable or disable the following clock edge. The enables are designed to be used with the data valid strobes from the GC3021A digital resampler and GC2011Adigital filter chips.

2.4 INPUT FORMAT

The input format circuit accepts complex data at the clock rate of the chip, or real data at twice the clock rate of the chip. The input format circuit outputs pairs of samples to the mixer circuit where the pair is either a complex data pair, or an even and odd time sample pair. A block diagram of the input circuit is shown in Figure 2.

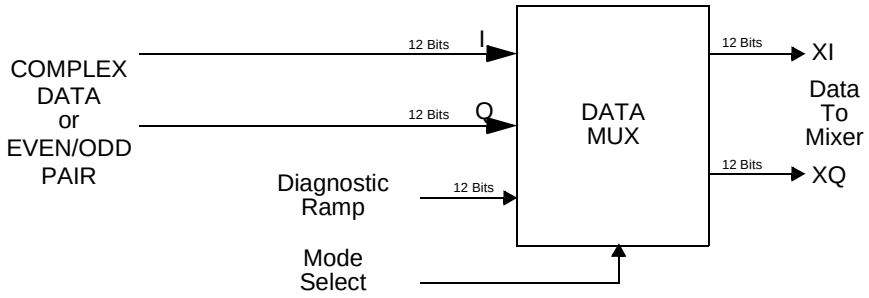


Figure 2. INPUT FORMAT CIRCUIT

The even/odd data inputs share pins with the I/Q complex data inputs. The I input pins are used as the even time inputs and the Q pins are used as the odd time inputs. The even samples are assumed to preceed the odd time samples. I.E., (X0, X2, X4, ...) are the even time samples, (X1, X3, X5,..) are the odd time samples.

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2.5 MIXER

The mixer multiplies the pairs of samples from the input format circuit by sines and cosines and outputs the results to the output format and the symbol offset circuits. A block diagram of the mixer circuit is shown in Figure 3.

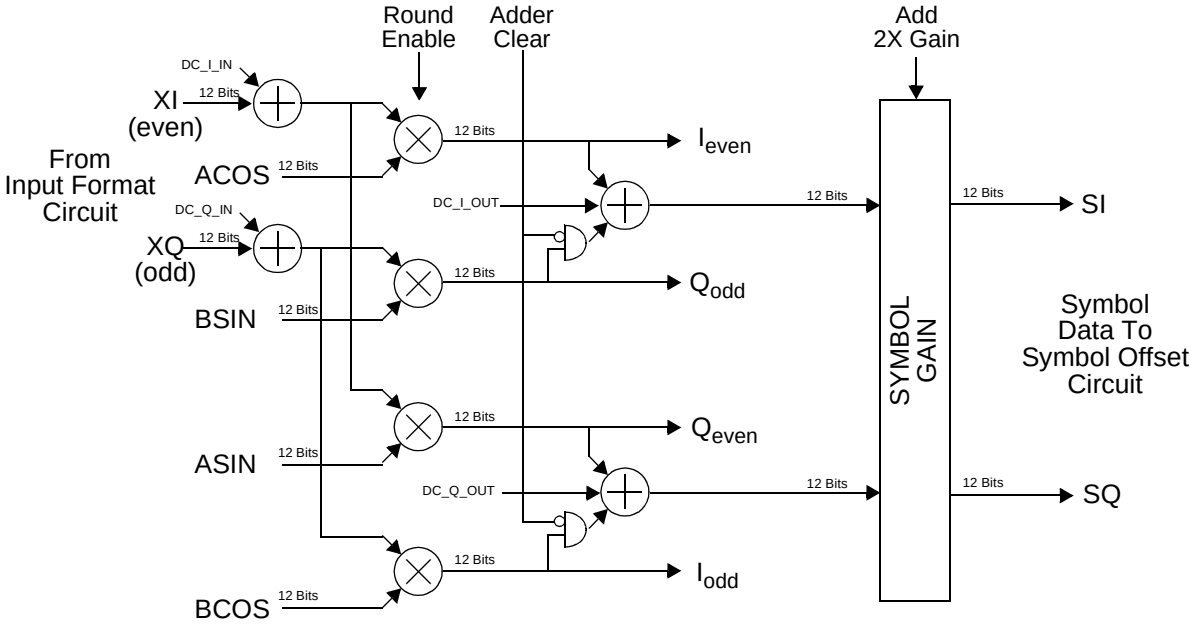


Figure 3. MIXER

The ACOS, BCOS, ASIN and BSIN values are generated by the NCO circuit. In the complex mode BCOS will equal ACOS and BSIN will equal minus ASIN. In the high speed mode the ASIN and ACOS values are the even time sine/cosine pairs and the BCOS and BSIN values are the odd time pairs. The lower 11 bits of the 23 bit multiplier products are either rounded off or truncated depending upon the state of the round enable control. The rounding is performed using the “round to even” technique[1]. The 12 bit products are passed to the output format circuit.

The adders sum the individual products to generate complex products. The adder outputs are saturated to 12 bits if the add causes overflow. The adder outputs pass through a gain circuit and then to the symbol offset circuit. The gain circuit, if it is enabled, doubles the data values. The gain outputs are saturated to plus or minus full scale if the gain causes overflow[2]. The adder clear control allows the I_{even} and Q_{even} mixer outputs, instead of the complex products, to be passed to the symbol gain circuit. This permits the user to capture the high speed mode’s even outputs in the snapshot RAM, or to use them in the phase error lookup circuit.

DC components before or after the mixer can be removed by adjusting the DC_I_IN, DC_Q_IN, DC_I_OUT and the DC_Q_OUT values. These values are added to the input and output data as shown in

1. When the fraction to be rounded is exactly 1/2, the round to even technique rounds up when the integer portion is odd and rounds down when it is even. This removes any DC bias in the rounding.
2. The input samples of QAM signals have an extra sign bit before the carrier is removed. The extra sign bit is needed because the square QAM constellation is spinning. Once carrier has been removed the extra sign bit can be removed by the gain circuit. This increases the resolution of the phase error RAM and simplifies the symbol mapping.

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Figure 3. The outputs from these adders are saturated to plus or minus full scale (12 bits) if overflow is detected.

2.6 SYMBOL ALIGN

The symbol align circuit is used in the carrier removal mode to process offset (or staggered) QPSK signals. The offset is removed by delaying the SI sample by one clock cycle so that it is paired with the next SQ sample. Every other SI and SQ pair is held for two clock cycles, effectively decimating the sample rate by two. The symbol offset circuit is controlled by the OFFSET and OFFSET_HOLD control bits described in Section 4.1 The symbol offset circuit is synchronized by the OFFSET_SYNC described in Section 4.2.

2.7 PHASE ERROR RAM

The the I and Q samples are passed to the phase error RAM. The phase error RAM uses the upper 7 bits of the I and Q values to look up the sign of the phase error for the sample. The phase error RAM contents are downloaded through the control interface. The phase error RAM outputs a 1 or a 0 depending upon whether the phase angle of the (I, Q) complex pair is greater than or smaller than the nearest decision point for the signal's constellation pattern. A "0" means that the phase angle needs to be increased to match the decision point and a "1" means it needs to be decreased. A block diagram of the phase error RAM circuit is shown in Figure 4.

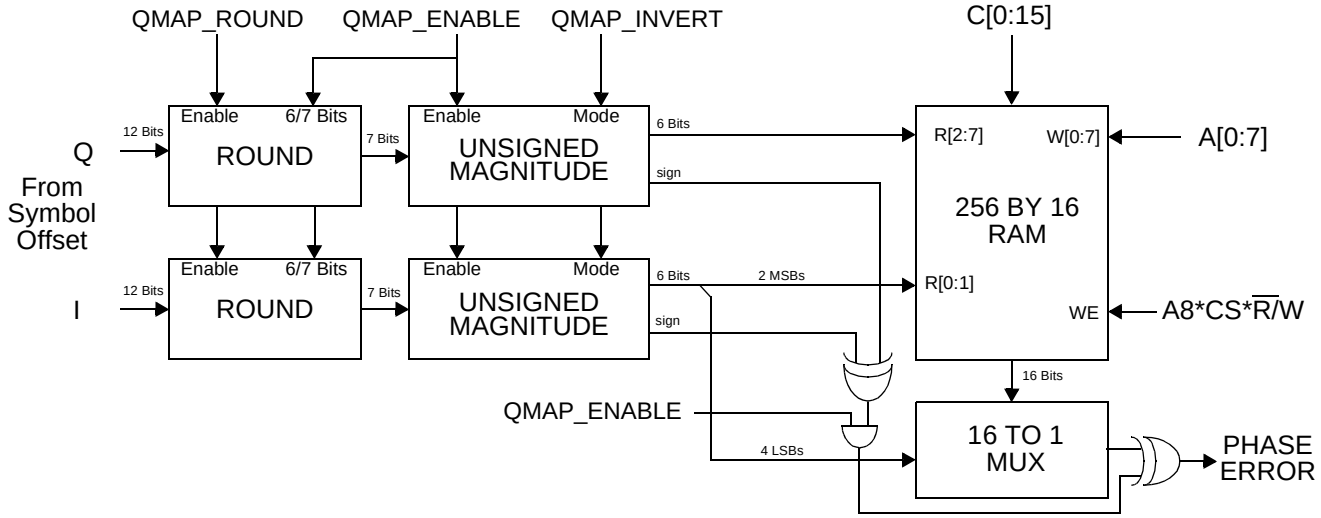


Figure 4. PHASE ERROR RAM

The round circuit rounds the 12 bit I and Q samples into the upper 6 or 7 bits, or, if rounding is disabled, truncates them. If the quadrant map (Qmap) mode is enabled the circuit rounds to 7 bits, otherwise it rounds to 6 bits. The rounding is performed using the round to even technique.

The rounded bits are passed to the unsigned magnitude circuit where, if Qmap is enabled, they are converted from 7 bit 2's complement signed numbers to 6 bit unsigned numbers. The conversion is performed using 2's complement negation unless the invert control is set. If the invert control is set, then the negation is performed by inverting the data bits (i.e., a 1's complement negation is used).

If Qmap is enabled the circuit outputs the 6 bit magnitude and the sign bit. If Qmap is turned off the circuit outputs the 6 bit signed number from the round circuit.

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The Qmap mode is used to map the I, Q complex pair into one quadrant for looking up the phase error. This is possible when the signal's constellation pattern has quadrant symmetry. If the pattern does not exhibit symmetry, then the quadrant map mode should not be used.

The 6 bit I and Q values are used to lookup the phase error in a 4096 by 1 bit memory. In the Qmap mode the phase error is inverted as necessary to map it back into the proper quadrant.

The memory is implemented using a 256 word by 16 bit RAM as shown in Figure 4. The RAM is loaded as 256 sixteen bit words mapped to addresses 256 to 511 of the control interface. The RAM is a write only memory.

The phase error is passed to the phase lock loop (PLL) circuit. The phase error is also output on the EOUT pin of the chip for external use.

2.8 PHASE LOCK LOOP

The phase error drives the PLL circuit shown in Figure 5.

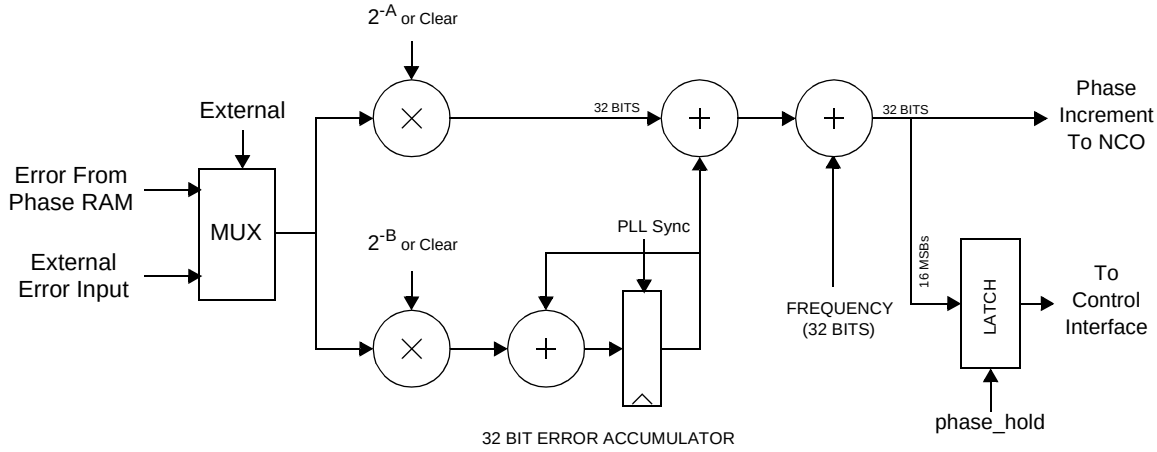


Figure 5. PLL CIRCUIT

The phase error can either come from an input pad or from the phase error RAM. The error is multiplied by the two constants 2^{-A} and 2^{-B}. These multipliers treat a phase error of "0" as +1 and a phase error of "1" as -1. The multipliers also have a clear mode so that 2^{-A} or 2^{-B} can be set to zero.

The tracking bandwidth and damping of the of the phase lock loop filter are set using the constants A and B. The filter will be critically damped when A is approximately one-half of B. When critically damped the tracking bandwidth and residual phase jitter of the loop are set by B. A small value for B results in a wide bandwidth with lots of jitter, but fast acquisition. A large value of B narrows the bandwidth and reduces the residual jitter, but increases the initial acquisition time. Values of B between 24 and 31 are suggested. Use 24 for initial acquisition and 31 for final tracking. The values of A and B are double buffered so that the loop bandwidth can be changed synchronous to an external sync signal.

Initial acquisition can be greatly aided by presetting the PLL to an estimated frequency offset. This is done by loading the frequency register with the estimated frequency.

In the mixer mode the PLL is turned off by clearing 2^{-A} and 2^{-B}, clearing the accumulator and setting the frequency register to the desired tuning frequency. The 32 bit frequency word is set to the desired frequency using the formula: $FREQ = \frac{Frequency}{Clock\ Rate} 2^{32}$, where "Frequency" is the desired

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frequency and “Clock Rate” is the chip’s clock rate. The frequency register is double buffered so that frequency changes can be made synchronous to external sync signals.

The upper 16 bits of the current phase increment is monitored by the phase increment register. The register tracks the current phase increment when the “hold” control is low and holds the last value when “hold” is high. The user may wish to monitor the phase increment in order to reinitialize the PLL after a loss of signal, or to determine when carrier lock has been achieved.

2.9 NCO

The PLL circuit generates a phase increment word which is used by the NCO to generate a sine/cosine sequence at the desired tuning frequency. The NCO circuit accumulates the phase and uses the upper 13 bits of the 32 bit accumulator to lookup 12 bit sines and cosines. A block diagram of the NCO circuit is shown in Figure 6.

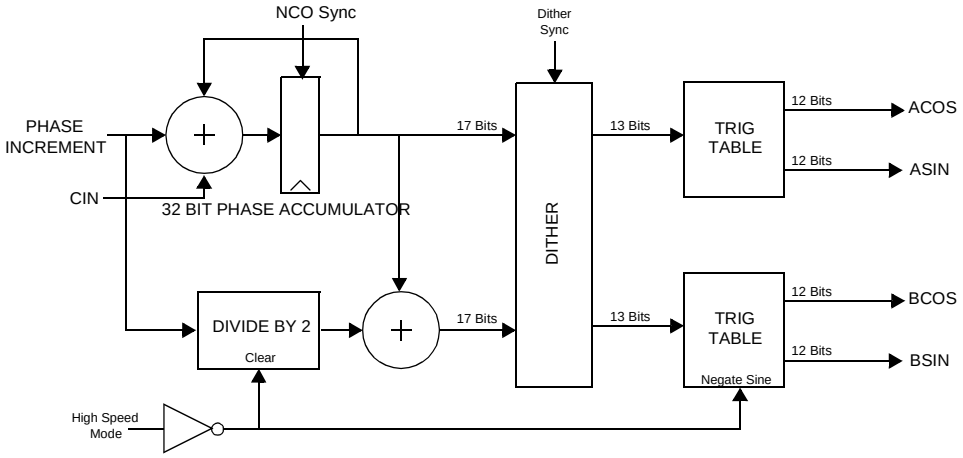


Figure 6. NCO CIRCUIT

The accumulator output plus one half the phase increment is used in the high speed mode[1] to look up the BCOS and BSIN values. This generates the proper “odd time” sine/cosine values needed in the high speed mode. The tuning range in the high speed mode is limited to +/- $F_{IN}/4$, where F_{IN} is thehigh speed input data rate. To tune to frequencies above $F_{IN}/4$, the user must negate the odd-time output samples (both I and Q). This mixes the output down by $F_{IN}/2$. For example, to mix down the frequency 0.3_{IN}, the user should set the tuning frequency to $+0.2F_{IN}$, and then negate the odd-time output data to give a final tuning of $(0.2F_{IN} - 0.5F_{IN}) = -0.3F_{IN}$.

The dither circuit adds a random value to the upper 17 bits of the accumulator output. The random number sequence is initialized to zero by the dither sync input. The dithering can be turned off by forcing the sync to be active. The BSIN output is negated if the high speed mode is not enabled.

2.10 SNAPSHOT RAM

The snapshot RAM is used to store blocks of 64 mixer and NCO outputs. The mixer outputs are the SI and SQ outputs shown in Figure 3. The NCO samples are the ACOS and ASIN values shown in Figure 3. The NCO samples are delayed to match the pipeline delay from the XI and XQ inputs to the SI and SQ

1. The high speed mode is the double rate real input mode, see Section 2.4

outputs. The snapshot can be programmed to store every sample, every other sample, every third sample, or every fourth sample. The rate control is primarily used when capturing samples of offset-QPSK data which is processed by the chip at twice the baud rate. Only every other sample of the offset-QPSK sample is of interest.

The snapshot can be triggered by the input syncs, the delayed input syncs, the sync counter's terminal count or the snap sync input. Once triggered, the snapshot start time can be delayed by up to 256 sample clocks, where the sample clock rate is dependant upon the snapshot rate control.

The snapshot RAM is a read only memory which is read using addresses 256 through 511 of the control interface. Addresses 256 through 319 read SI, addresses 320 through 383 read SQ, addresses 384 through 447 read ASIN, and addresses 448 through 511 read ACOS. The 12 bit values are sign extended to 16 bits in the control interface.

2.11 OUTPUT FORMAT

The chip has four 12 bit output ports labeled YA, YB, YC, and YD. Each port can be individually configured to output mixer results (I_{even}, Q_{even}, I_{odd}, Q_{odd}), or symbol and NCO samples. The symbol and NCO samples are the snapshot RAM inputs (SI, SQ, sine, cosine). The output selection is shown in Table 1 below:

Table 1: OUTPUT SELECTION

OUTPUT PORT	OUTPUT SELECT	
	0	1
YA	I_{even}	SI
YB	Q_{even}	SQ
YC	I_{odd}	cosine
YD	Q_{odd}	sine

The YA, YB, YC and YD outputs can be rounded to 12, 10 or 8 bits and can be masked to a desired number of bits through the use of four 12 bit mask words. The masks are bitwise ANDed with the output words to selectively clear the output bits.

Output enable controls are provided to individually turn off these outputs.

2.12 DATA DELAYS

The data delay through the chip in input clock cycles is shown in Table 2 below.

Table 2: DATA DELAYS

FROM	TO	DELAY	MODE
I, Q	SI, SQ	15	OUTSEL=1
I, Q	I, Q (even/odd)	13	OUTSEL=0

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2.13 POWER DOWN MODES

The chip has a power down and clock loss detect circuit. This circuit detects if the clock is absent long enough to cause dynamic storage nodes to lose state. If clock loss is detected, an internal reset state is entered to force the dynamic nodes to become static. The control registers are not reset and will retain their values, but any data values within the chip will be lost. When the clock returns to normal the chip will automatically return to normal. In the reset state the chip consumes only a small amount of standby power. The user can select whether this circuit is in the automatic clock-loss detect mode, is always on (power down mode), or is disabled (the clock reset never kicks in) using the POWER_DOWN control bits in address 1.

NOTE: The chip is in the power down mode when power is applied, and must be enabled by setting the power down mode to "2" in register 1.

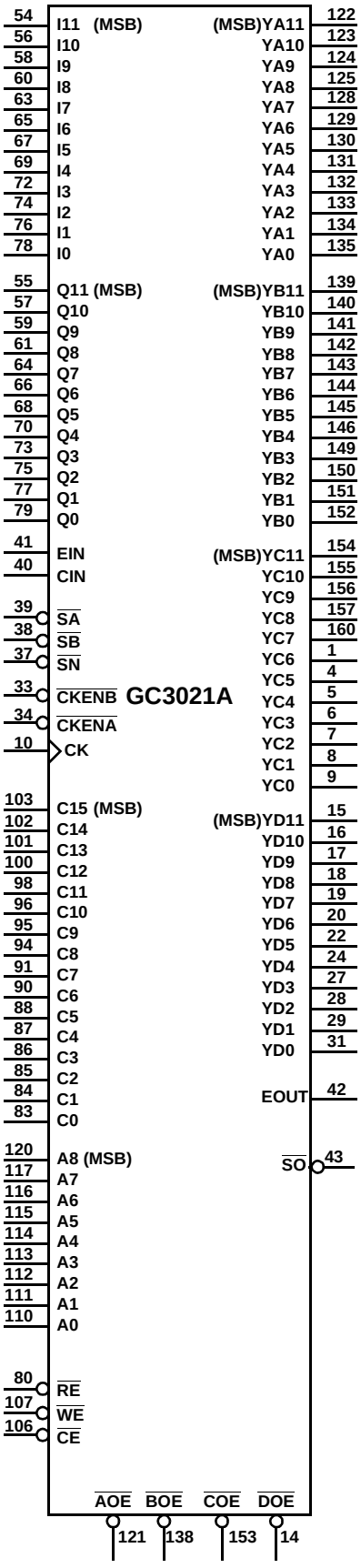
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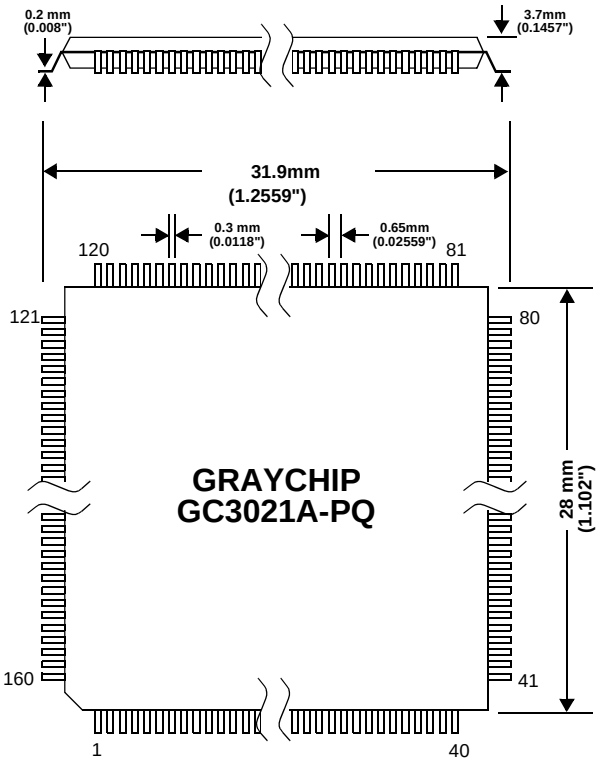
2.14 DIAGNOSTICS

The sync counter can be used as an input sync and data source in order to perform diagnostics. The diagnostic outputs are captured in the snapshot RAM and compared with predicted results. The whole chip except for the I/O pads, the high speed input circuit and the output format circuit can be checked this way. Section 6.6 tabulates the diagnostic configurations and their expected snapshot outputs.

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3.0 PACKAGING





160 PIN PLASTIC QUAD FLAT PACK CHIP CARRIER

VCC PINS: 3,12,13,23,26,32,36,44,47, 48,81,89,93,97,104,108,118,126,136,147,158

GND PINS: 2,11,21,25,30,35,45,46,82,92,99,105,109,119,127,137,148,159

UNUSED PINS: 53, 62, 71, 49, 50, 51, 52

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

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3.1 PIN DESCRIPTIONS

SIGNAL	DESCRIPTION
I[0:11]	**IN-PHASE INPUT DATA.** *Active high* The 12 bit two's complement input samples for the I half of the complex input. New samples are clocked into the chip on the rising edge of the clock.
Q[0:11]	**QUADRATURE INPUT DATA.** *Active high* The 12 bit two's complement input samples for the Q-half of the complex input. New samples are clocked into the chip on the rising edge of the clock.
CIN	**NCO CARRY INPUT.** *Active high* The carry input to the phase accumulator in the NCO. The CIN input can be used to increase the tuning resolution of the NCO. This signal is clocked into the chip on the rising edge of the clock. The CIN input is cleared by the chip during diagnostics.
EIN	**PHASE ERROR INPUT.** *Active high* This input can be used as the error input into the PLL circuit. This signal is clocked into the chip on the rising edge of the clock.
$\overline{\textbf{SA}}$,$\overline{\textbf{SB}}$	**SYNC INPUTS**. *Active low* The sync inputs to the chip. All timers, accumulators, and control counters are, or can be, synchronized to these syncs. The syncs are clocked into the chip on the rising edge of the clock.
$\overline{\textbf{SN}}$	**SNAPSHOT SYNC**. *Active low* The snapshot sync is provided to synchronously start the data snapshot. This signal is clocked into the chip on the rising edge of the clock.
CK	**CLOCK INPUT.** *Active high* The clock input to the chip. The **I**, **Q**, $\overline{\textbf{SA}}$, $\overline{\textbf{SB}}$, $\overline{\textbf{SN}}$, $\overline{\textbf{CKENA}}$, $\overline{\textbf{CKENB}}$, **EIN** and **CIN** signals are clocked into the chip on the rising edge of this clock. The **YA**, **YB**, **YC**, **YD**, **EOUT** and $\overline{\textbf{SO}}$ signals are clocked out on the rising edge of this clock.
$\overline{\textbf{CKENA}}$, $\overline{\textbf{CKENB}}$	**CLOCK ENABLE INPUTS.** *Active low* The clock enable inputs to the chip. These signals are gated with **CK** to generate the chip's internal clock. $\overline{\textbf{CKENA}}$ and $\overline{\textbf{CKENB}}$ are clocked into the chip on the rising edge of **CK** and will enable or disable the following clock edge. A low level on both $\overline{\textbf{CKENA}}$ and $\overline{\textbf{CKENB}}$ enables the clock edge.
YA[0:11] **YB[0:11]** **YC[0:11]** **YD[0:11]**	**YA OUTPUT DATA**. *Active high* **YB OUTPUT DATA**. *Active high* **YC OUTPUT DATA**. *Active high* **YD OUTPUT DATA**. *Active high* These pins output the complex mixer or symbol outputs. The bits are clocked out on the rising edge of the clock.
$\overline{\textbf{AOE}}$,$\overline{\textbf{BOE}}$,$\overline{\textbf{COE}}$,$\overline{\textbf{DOE}}$	**OUTPUT ENABLES**. *Active low* The **YA, YB, YC** and **YD** output pins are put into a high impedance state when these pins are high. $\overline{\textbf{AOE}}$ controls the **YA** output pins. $\overline{\textbf{BOE}}$ controls the **YB** output pins. $\overline{\textbf{COE}}$ controls the **YC** output pins. $\overline{\textbf{DOE}}$ controls the **YD** output pins.

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EOUT	**PHASE ERROR OUT**. *Active high* The phase error RAM output is clocked out of the chip on this pin. This signal is made available mostly for diagnostic purposes.
$\overline{\text{SO}}$	**SYNC OUT**. *Active low* This signal is either one of the input syncs, the one shot sync **$\overline{\text{OS}}$**, or the internal counter's terminal count strobe **$\overline{\text{TC}}$**.
C[0:15]	**CONTROL DATA I/O BUS**. *Active high* This is the 16 bit control data I/O bus. Control register contents are loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{\text{CE}}$** and **$\overline{\text{RE}}$** are low and **$\overline{\text{WE}}$** is high.
A[0:8]	**CONTROL ADDRESS BUS**. *Active high* These pins are used to address the control registers, phase error RAM and the snapram memory within the chip.
$\overline{\text{WE}}$, **$\overline{\text{RE}}$**	**READ/$\overline{\text{WRITE}}$ CONTROL**. *Active low* These pin determines if the control bus cycle is a read or write operation.
$\overline{\text{CE}}$	**CHIP ENABLE**. *Active low* This control strobe enables the chip for read or write operations.
VCC	**SUPPLY VOLTAGE.** *Fixed voltage* The power supply pins.
GND	**CHIP GROUND.** *Fixed voltage* The power supply ground pins.

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4.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 14 sixteen bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{\text{CS}}$**, **R/$\overline{\text{W}}$**, **A[0:8]**, and **C[0:15]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	MODE_REG	8	OUTPUT_REGA
1	SYNC_REG0	9	OUTPUT_REGB
2	SYNC_REG1	10	OUTPUT_REGC
3	DELAY_REG	11	OUTPUT_REGD
4	COUNTER_REG0	12	SNAP_REG
5	PLL_REG	13	PHASE_REG
6	FREQ_REG0	14	ONE_SHOT
7	FREQ_REG1	15	TEST_OUT
16	DC_I_IN		
17	DC_Q_IN		
18	DC_I_OUT		
19	DC_Q_OUT		

20 to 255	unused
256 to 511	Snapshot memory (read only)
256 to 511	Phase Error memory (write only)

The DC offset registers contain two's complement values. Only the 12 LSBs are used.

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

Suggested default settings for using the chip in carrier removal applications is given for each register.

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4.1 MODE CONTROL REGISTER

This register contains the mode control bits. The suggested default value is 5280 (HEX).

ADDRESS 0: MODE_REG

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	INPUT[0:1]	This two bit field controls the input data selection. The input modes are: INPUT DESCRIPTION 0 Complex data input 1 High speed real data input 2 Diagnostic ramp input 3 Zero input
2-6	R/W	-	unused
7	R/W	MIXER_ROUND	Round the mixer multiplier products to 12 bits. The products are truncated to 12 bits if this control is low.
8	R/W	ADDER_CLEAR	Clears one input to the adder in the mixer circuit to allow the I_{even} and Q_{even} outputs to be routed to the symbol offset circuitry. See Section 2.5.
9	R/W	2X_GAIN	Enables the 2X gain circuit in the mixer circuit.
10	R/W	OFFSET	Delays the I sample in the symbol offset circuit by one clock cycle relative to the Q sample.
11	R/W	OFFSET_HOLD	Samples and holds every other I,Q pair in the symbol offset circuit. The OFFSET_SYNC mode (See Section 4.2) determines how the sample and hold timing is synchronized to the input data.
12	R/W	QMAP_ENABLE	Enables the quadrant map mode. This mode maps the I,Q pairs into the first quadrant for phase error lookup when this mode is selected. The error is then mapped back to the correct quadrant after it is looked up in the phase error memory.
13	R/W	QMAP_ROUND	Round instead of truncate the I,Q samples in the phase error circuit. If QMAP_ENABLE is set the values are rounded into the 7 MSBs, otherwise they are rounded to the 6 MSB.
14	R/W	QMAP_INVERT	Convert negative numbers to positive numbers in the Qmap mode by inverting the data bits (1's complement negation) rather than negating them.
15	R/W	NCO_MODE	Turns on the high speed NCO mode. Must be high for the high speed double rate input mode, low otherwise.

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4.2 SYNC CONTROL REGISTERS

Control registers SYNC_REG0 and SYNC_REG1 determine how the circuits within the chip are synchronized. Each circuit which requires synchronization can be configured to be synchronized to the sync inputs **(SA** and **SB**), to the delayed versions of these syncs (**DSA** and **DSB**), to the terminal count of the internal counter (**TC**), or to the one-shot strobe (**OS**). The sync to each circuit can also be set to be always on or always off. Each circuit is given a three bit sync mode control which is defined as:

Table 3: SYNC MODES

MODE	SYNC DESCRIPTION
0	"0" (never asserted)
1	SA
2	SB
3	DSA
4	DSB
5	TC
6	OS
7	"1" (always asserted)

NOTE: the internal syncs are active high. The **$\overline{\text{SA}}$** and **$\overline{\text{SB}}$** inputs have been inverted to be the active high syncs **SA** and **SB**.

The suggested default setting for SYNC_REG0 is to sync everything to SA, value = 0249 (HEX).

ADDRESS 1: SYNC_REG0

BIT	TYPE	NAME	DESCRIPTION
0-2 (LSBs)	R/W	COUNT_SYNC	The counter sync selection
3-5	R/W	OUTPUT_SYNC	The selected sync is inverted and output on the **$\overline{\text{SO}}$** pin.
6-8	R/W	OFFSET_SYNC	The symbol offset sync.
9-11	R/W	SNAP_SYNC	The snapshot memory can be triggered by this sync.
12	R/W	-	unused
13	R/W	USE_CLK_EN	The clock enables **$\overline{\text{CKENA}}$** and **$\overline{\text{CKENB}}$** are ignored when this bit is low.
14,15	R/W	POWER_DOWN	These bits control the power down and keep alive circuit. POWER_DOWN — MODE 0,1 — Power down 2 — Clock loss detect mode 3 — Clock loss detect off

The USE_CLK_EN and POWER_DOWN bits initialize to zero upon power up. This puts the chip in the power down mode to prevent a current surge if there is no clock provided. See Section 2.13 for details.

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The suggested default value for SYNC_REG1 is 7DF7 (HEX) which is to always sync AB_SYNC, FREQ_SYNC and DITHER_SYNC (turns dithering off) and to sync PLL_SYNC and NCO_SYNC with the oneshot strobe.

ADDRESS 2: SYNC_REG1

BIT	TYPE	NAME	DESCRIPTION
0-2 (LSBs)	R/W	AB_SYNC	The PLL circuit accepts new A and B values when the sync is asserted.
3-5	R/W	PLL_SYNC	The PLL accumulator is cleared by this sync.
6-8	R/W	FREQ_SYNC	The PLL accepts the new FREQ value from the FREQ registers when this sync is asserted.
9-11	R/W	NCO_SYNC	The NCO accumulator is cleared by this sync.
12-14	R/W	DITHER_SYNC	The dither value circuit is cleared by this sync.
15 (MSB)	R/W	-	unused

4.3 DELAY CONTROL REGISTER

The **DSA** and **DSB** syncs are generated by delaying the **SA** and **SB** sync inputs by (2+DELAY) clocks where DELAY ranges from 0 to 255. The suggested default is zero.

ADDRESS 3: DELAY_REG

BIT	TYPE	NAME	DESCRIPTION
0-7 (LSBs)	R/W	DELAY_A	The DELAY value for **DSA**.
8-15 (MSBs)	R/W	DELAY_B	The DELAY value for **DSB**.

4.4 COUNTER CONTROL REGISTER

The internal counter counts in cycles of 16*(COUNT+1) clocks by counting down from (16*COUNT+15) to zero and starting over again. The counter emits a terminal count (TC) each time it reaches zero. The suggested default is 00FF (HEX) which sets a counter cycle of 4096.

ADDRESS 4: COUNT_REG

BIT	TYPE	NAME	DESCRIPTION
0-15	R/W	COUNT	The counter period is 16*(COUNT+1) clocks.

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4.5 PLL CONTROL REGISTER

The phase lock loop (PLL) phase hold control and filter coefficients are stored in this register. The suggested default is 028A (HEX) which sets A=10 and B=20 for acquisition, and 038e (HEX) which sets A=14 and B=28 for tracking.

ADDRESS 5: PLL_REG

BIT	TYPE	NAME	DESCRIPTION
0-4	R/W	A[0:4]	The 5 bit "A" coefficient. See Figure 5. The phase error is multiplied by 2^{-A} for A equal to 1 through 31, and is multiplied by 0 for A equal to 0.
5-9	R/W	B[0:4]	The 5 bit "B" coefficient. See Figure 5. The phase error is multiplied by 2^{-B} for B equal to 1 through 31, and is multiplied by 0 for B equal to 0.
10	R/W	EXT_ERROR	Use the **EIN** input as the error input to the PLL circuit. **EIN** = 0 adds to the phase, **EIN** = 1 subtracts.
11-14	R/W	-	unused
15 (MSB)	R/W	PHASE_HOLD	The phase register tracks the value of the phase increment when this bit is low and holds the last value when this bit is high.

The A and B coefficients stored in this register are not used until the AB_SYNC is asserted as described in Section 4.2.

4.6 FREQUENCY WORD REGISTERS

Registers 6 and 7 contain the 32 bit frequency tuning word. The frequency word is added into the PLL output as shown in Figure 4. Bit 0 is the LSB, bit 31 is the MSB. The suggested default is zero.

ADDRESS 6: FREQ_REG0

BIT	TYPE	NAME	DESCRIPTION
0-15	R/W	FREQ[0:15]	16 LSBs of the frequency word

ADDRESS 7: FREQ_REG1

BIT	TYPE	NAME	DESCRIPTION
0-15	R/W	FREQ[15:31]	16 MSBs of the frequency word

The tuning frequency is specified using the formula:

$$\text{FREQ} = \frac{\text{Frequency}}{\text{Clock Rate}} 2^{32}$$

where "Frequency" is the desired tuning frequency, and "clock rate" is the chip's clock rate. The FREQ value stored in these registers are transferred to the PLL circuit when the FREQ_SYNC is asserted as described in Section 4.2.

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4.7 OUTPUT CONTROL REGISTERS

Registers 8, 9, 10 and 11 contain the four output format control words. Each register is identical. OUTPUT_REGA controls output YA, OUTPUT_REGB controls output YB, OUTPUT_REGC controls output YC and OUTPUT_REGD controls output YD. The suggested default is 1FFF.

ADDRESS 8: OUTPUT_REGA
ADDRESS 9: OUTPUT_REGB
ADDRESS 10: OUTPUT_REGC
ADDRESS 11: OUTPUT_REGD

BIT	TYPE	NAME	DESCRIPTION
0-11	R/W	MASK	12 Bit output mask. MASK is bitwise anded with the output sample. Bit 0 is the LSB, bit 11 is the MSB.
12	R/W	OUTPUT_SEL	Selects which signal is output on this port. See Table 2 in Section 2.11.
13	R/W	RND_8	Round to 8 bits
14	R/W	RND_10	Round to 10 bits
15	R/W	-	Unused

The RND_8 and RND_10 controls are used to round the 12 bit output values to 8 or 10 bits. Only one control should be high.

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4.8 SNAPSHOT CONTROL REGISTER

Registers 12 controls the snapshot memory. The suggested default is 0002 (HEX).

ADDRESS 12: SNAP_REG

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSB)	R/W	TRIGGER	This control sets the trigger condition which will start a snapshot once the ARMED bit is set. The trigger conditions are to start: TRIGGER DESCRIPTION 0 immediately, 1 when the **$\overline{SN}$** strobe is received, 2 when the SNAP_SYNC is received (See Section 4.2), 3 never
2	R/W	ARMED	The user sets this bit to arm the snapshot memory so that it will start on the next trigger condition. The chip clears this bit when the trigger occurs.
3	R/W	DONE	This bit goes high when the snapshot is complete.
4,5	R/W	SNAP_RATE	Determines the rate at which samples are stored according to: SNAP_RATE DESCRIPTION 0 every clock, full rate samples 1 every other clock, half rate samples 2 every 3rd clock, third rate samples 3 every 4th clock, quarter rate samples.
6,7	R/W	-	unused
8-15 (MSB)	R/W	SNAP_DELAY	Delay from snapshot trigger until the start of snapshot. The delay is: SNAP_DELAY*(SNAP_RATE+1) clock cycles where SNAP_DELAY ranges from 0 to 255.

4.9 PHASE REGISTER

Register 13 is a read only register used to monitor the upper 16 bits of the NCO's phase increment. See PHASE_HOLD in Section 4.5.

4.10 ONE SHOT ADDRESS

The one shot pulse is generated on the **$\overline{OS}$** pin by writing to address 14. This is a write-only address. The data written to it is irrelevant.

4.11 TEST OUTPUT REGISTER

Register address 15 is a read only port used to monitor the powerdown and clock loss modes. Bit 0 is low if the chip is in power down, and bit 1 is low if clock loss has been detected. Normally both bits will read as 1.

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5.0 SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	4.0	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.7	V_{CC}+0.7	V	
Storage Temperature	T_{STG}	-65	150	^{o}C	
Lead Soldering Temperature (10 seconds)			300	^{o}C	
Clock Rate	F_{CK}	1		KHz	1

Notes:

1. Below 1 KHz the clock loss detect circuit may power down the chip. If the clock loss detect circuit is disabled (address 1, bits 14 and 15) and the clock is stopped, the chip may draw up to one Amp of power supply current for approximately 10 seconds. After 10 seconds the current will go down to below 50 mAmps.

5.2 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.0	3.6	V	
Temperature Ambient, no air flow	T_A	-40	+85	^{o}C	1
Junction Temperature	T_J		125	^{o}C	1

Notes:

1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 3 below.

5.3 THERMAL CHARACTERISTICS

Table 6: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC3021A-PQ	UNITS
		0.5 Watts	
Theta Junction to Ambient	θja	30	^{o}C/W
Theta Junction to Case	θjc	10	^{o}C/W

Note: Air flow will reduce θ**ja** and is highly recommended.

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5.4 DC CHARACTERISTICS

All parameters are industrial temperature range of 0 to 85 ^{o}C ambient unless noted.:

Table 7: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		UNITS	NOTES
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	1
Voltage input high	V_{IH}	2.0		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50		uA	2
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	2
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4	3.3	V	2
Data input capacitance (All inputs except **CK** and **C[0:15]**)	C_{IN}	Typical 4		pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10		pF	1
Control data capacitance (**C[0:7]** I/O pins)	C_{CON}	Typical 6		pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{o}C for the given specification.

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5.5 AC CHARACTERISTICS

Table 8: AC Characteristics (0 TO +85^{o}C Ambient, unless noted)

PARAMETER	SYMBOL	3.3V +/- 5%		UNITS	NOTES
		MIN	MAX		
Clock Frequency	F_{CK}	0.01	100	MHz	2, 3, 4
Clock low period (Below V_{IL})	t_{CKL}	3		ns	1
Clock high period (Above V_{IH})	t_{CKH}	5		ns	1
Data setup before **CK** goes high	t_{SU}	4		ns	1
Data hold time after **CK** goes high	t_{HD}	2		ns	1
Data output delay from rising edge of **CK**.	t_{DLY}	2	8	ns	1, 5
Control Setup before $\overline{\textbf{CE}}$ goes low (**A**, **RE, WE** during read, and **A**, **RE, WE** , **C** during write)	t_{CSU}	5		ns	1
Control hold after $\overline{\textbf{CE}}$ goes high (**A**, **RE, WE** during read, and **A**, **RE, WE**, **C** during write)	t_{CHD}	5		ns	1
Control strobe ($\overline{\textbf{CE}}$) pulse width (Write operation)	t_{CSPW}	20		ns	1,6
Control output delay $\overline{\textbf{CE}}$ low to **C** (Read Operation)	t_{CDLY}		20	ns	1,6
Control tristate delay after $\overline{\textbf{CS}}$ goes high	t_{CZ}		5	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 1KHz)	I_{CCQ}		200	uA	1
Supply current (F_{CK} =100MHz)	I_{CC}		150	mA	1, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 85 deg C for the given specification.
3. Temperature range is verified by lot sampling.
4. The chip may not operate properly at clock frequencies below MIN and above MAX.
5. Current load is 2ma. Delays are measured from the rising edge of the clock to the output level rising above V_{IH} or Falling below V_{IL}.
6. Capacitive output load is 80pf.
7. Current changes linearly with voltage and clock speed. Icc (MAX) $= \left(\frac{VCC}{3.3V}\right)\left(\frac{F_{CK}}{100M}\right)150mA$

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6.0 APPLICATION NOTES

6.1 POWER AND GROUND CONNECTIONS

The GC3021A chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC3021A chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC3021A chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC3021A chip may not operate properly if these power and ground guidelines are violated.

6.2 STATIC SENSITIVE DEVICE

The GC3021A chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

6.3 REDUCED VOLTAGE OPERATION

The power consumed by the GC3021A chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements.

6.4 HIGH SPEED MIXER

The GC3021A chip can be used with two GC2011 filter chips to implement a high speed quadrature down converter capable of accepting data rates up to 200 MHz, tuning to a desired frequency and outputting 100 MHz complex data. A block diagram of the suggested configuration is shown below:

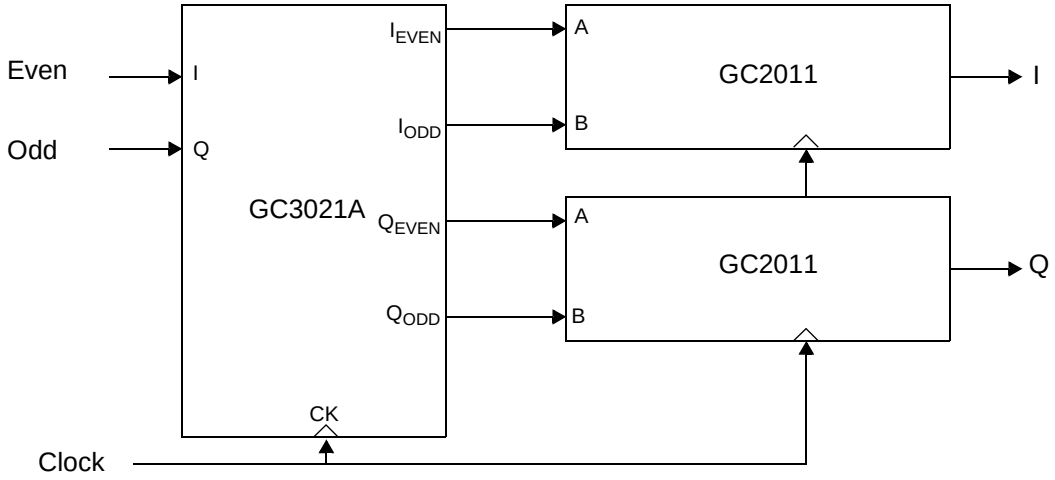


Figure 7. HIGH SPEED MIXER EXAMPLE

The GC2011 Digital filter chips are used in a decimate by two, double rate in, full rate out mode.

6.5 QAM DEMODULATOR

The GC3021A chip can be used for carrier removal high speed digital modems. Examples include digital microwave links and HDTV systems. For details in using the GC3021A chips in a digital modem contact GRAYCHIP for the application note: BUILDING DIGITAL PSK AND QAM DEMODULATORS, August 17, 1994.

6.6 DIAGNOSTICS

Eight diagnostic tests are defined on the following pages. Note that the CIN input to the chip must be grounded.

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```
# GC3021A diagnostic test A
#
# This test uses odd parity map.
#
for (i=0;i<256;i++) write (base+i) odd_parity(i);
#
# where odd_parity(i) is 0x9669 if "i" contains an odd number of bits
# and is 0x6996 otherwise (e.g., base + 0 = 0x6996, base + 1 = 0x9669, etc)

# control register settings:
write  0 0x0002
write  1 0x8b6e
write  2 0x5fef
write  3 0x0000
write  4 0x00bf
write  5 0x0082
write  6 0x0000
write  7 0x0000
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0000
write 17 0x0000
write 18 0x0000
write 19 0x0000

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0xfa85 0xf800 0x01f0 0xf800 0xfa7d 0xf8f5 0xfa73 0xfffc
0xf800 0xfffc 0xf800 0x03d5 0xf800 0x071f 0x07ff 0x07ff
0x01f6 0x07ff 0x01fa 0x07ff 0x01fb 0x07ff 0x07ff 0x0740
0x05b1 0x0745 0x05b5 0x074b 0x05bb 0x0752 0x05c0 0x0757
0x07ff 0x0000 0xfa34 0xf800 0xf800 0xf894 0xfdf0 0xf800
0x020b 0xf800 0xf800 0xf885 0xfa1a 0xfbec 0xfa16 0xfbe9
0xf800 0xfbe8 0xfde8 0xf800 0xfde6 0xf800 0xfde3 0xf800
0xfde3 0xf800 0xfddf 0xfffc 0x0605 0x07ff 0x07ff 0x07b7

0xf800 0xfc36 0xf800 0x03ca 0xf800 0x0708 0x07ff 0x07ff
0xfe09 0x07ff 0x01f1 0x07ff 0x01f3 0x0722 0x01f8 0xfc23
0x07ff 0xfc1f 0x07ff 0xfc1c 0x07ff 0xfc17 0xfa51 0xf8c1
0x07ff 0xf8ba 0x07ff 0xf8b4 0x07ff 0xf8af 0x07ff 0xf8a8
0x05c8 0xf800 0xf800 0xfbfd 0x0208 0x0767 0x07ff 0xfffc
0x07ff 0xfbf3 0xfa1e 0xf882 0x07ff 0x07ff 0x07ff 0x07ff
0xfa11 0x07ff 0x07ff 0xfbe4 0x07ff 0xfbe0 0x07ff 0xfbdc
0x07ff 0xfbdb 0x07ff 0x07ff 0x07ff 0x042b 0xfde1 0xf848

0x0190 0xfcf2 0x06a8 0xf89d 0x0191 0xf801 0xf828 0xfa57
0xfb90 0xfa57 0xf95c 0xfcef 0xf95c 0xfffe 0x0471 0x0762
0xfb8d 0x0762 0xfb8e 0x0762 0xfb8e 0x0763 0x07d7 0x07ff
0xfe6f 0x07ff 0xfe6f 0x07ff 0xfe70 0x07ff 0xfe70 0x07ff
0x018e 0x05a8 0x0190 0xfcf3 0xf95b 0xf801 0xf958 0xfa5a
0xfb8e 0xfcf3 0xfe73 0x0002 0xf828 0xf89c 0xf828 0xf89c
0xfe72 0xf89d 0xf959 0xfcf2 0xf959 0xfcf3 0xf958 0xfcf3
0xf959 0xfcf2 0xf958 0xfa57 0xfe6f 0x030d 0x06a5 0x07ff

0x07d7 0x0763 0x0470 0x0310 0x07d7 0x0001 0xfe73 0xfa5a
0x06a8 0xfa5a 0x0473 0xf89e 0x0473 0xf801 0xf959 0xfcef
0xf95c 0xfcef 0xf95b 0xfcef 0xf95b 0xfcf0 0xfe70 0xfffe
0xf829 0xffff 0xf829 0xffff 0xf829 0xfffe 0xf829 0xffff
0xf828 0x05a7 0x07d7 0x0764 0x0472 0x0002 0xfb90 0x05a9
0xf95b 0x0764 0x07d8 0x07ff 0xfe72 0xfcf3 0xfe72 0xfcf3
0x07d8 0xfcf2 0xfb8f 0x0763 0xfb8f 0x0764 0xfb90 0x0764
0xfb8f 0x0763 0xfb90 0xfa5a 0xf829 0xf89c 0xfb8e 0xffff
```


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```
# GC3021A diagnostic test B
#
# use the odd parity map, see testA

# control register settings:
write  0 0x0202
write  1 0x8b6e
write  2 0x5fef
write  3 0x0000
write  4 0x00ff
write  5 0x0044
write  6 0xaaaa
write  7 0xeaaa
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0fff
write 17 0x0400
write 18 0x0001
write 19 0x0bff

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0xfe5c 0xfcd4 0x0622 0xfa8a 0x018a 0x0352 0xf9c6 0xfaca
0x0170 0xfc4c 0xf9b0 0xfc52 0xfeaa 0x03a6 0x014a 0xfa8e
0xf98e 0xfc4a 0x067c 0xfa94 0x0126 0x0388 0xfe80 0xfc16
0xf97e 0xfa42 0xf978 0xfa96 0xf94e 0xfc96 0xf96e 0xfbd4
0x00d8 0x043c 0x069c 0x0450 0xff42 0xfaa0 0x00b0 0x0560
0xfdee 0xf9c8 0xf900 0x0646 0x06b8 0x055c 0x0718 0xfaa4
0xf8de 0xfce2 0x0260 0xfaa4 0xf8c8 0xf96e 0x004a 0x0558
0x0750 0xf94e 0x02a4 0x02fa 0x0766 0x02f2 0x0016 0x0554

0xf800 0xfd72 0xf800 0xf800 0xfe2a 0xf800 0xf97a 0xfbba
0xfe40 0xf800 0xf960 0xf800 0xf800 0xfd5e 0xfe62 0xfb9a
0xf938 0xfd6a 0xf800 0xf800 0xfe82 0xfd9a 0xfe78 0xfd64
0xf800 0xfb76 0xf800 0xf800 0xf8ee 0xf800 0xf800 0xfd62
0xfec4 0xf800 0xf9dc 0xf800 0xf800 0xf800 0xfee6 0xfc6c
0xfeaa 0xfb38 0xf892 0xf800 0xfa2c 0xfca0 0xf800 0xf800
0xf86e 0xf800 0xf800 0xf800 0xf852 0xfb0c 0xff40 0xfcf4
0xf800 0xfafe 0xf800 0xfebc 0xf800 0xfecc 0xff6c 0xfd38

0x07fb 0xfaba 0xff78 0x0603 0xf805 0x0544 0x0088 0xfd70
0xf805 0x0794 0x0088 0x0793 0x07fb 0xf86c 0xf805 0xfd71
0x0089 0xfabc 0xff7a 0x0605 0xf805 0xf86d 0xf8d5 0xfabd
0x038b 0xfd70 0x038b 0x0603 0x0086 0x0793 0x0389 0xfaba
0xf805 0x0546 0xfc77 0x0543 0x07fb 0x0605 0xf805 0xf9fb
0xf8d5 0xfd71 0x0088 0x028f 0xfc77 0xf9fb 0xff7a 0x0605
0x0086 0x0793 0x072b 0x0603 0x0088 0xfd70 0xf805 0xf9fb
0xff7a 0xfd70 0x072b 0xf86d 0xff77 0xf86d 0xf805 0xf9fb

0xff78 0x0603 0xf805 0x0546 0x0088 0xf9fb 0x07fb 0x0793
0x0089 0x028f 0x07fb 0x0290 0xff78 0xfd71 0x0088 0x0794
0x07fb 0x0605 0xf805 0x0544 0x0086 0xfd70 0x0389 0x0606
0x072b 0x0793 0x072b 0x0546 0x07fb 0x0290 0x072b 0x0603
0x0086 0xf9fd 0xf8d5 0xf9fa 0xff7a 0x0544 0x0089 0xfabc
0x038b 0x0794 0x07fb 0xf86c 0xf8d5 0xfabc 0xf805 0x0544
0x07fb 0x0290 0xfc77 0x0546 0x07fb 0x0793 0x0089 0xfabc
0xf805 0x0793 0xfc75 0xfd70 0xf805 0xfd70 0x0088 0xfabc
```


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```
# GC3021A diagnostic test C
#
# use the odd parity map, see testA

# control register settings:
write  0 0x0e02
write  1 0x8b6e
write  2 0x5bff
write  3 0x0000
write  4 0x003f
write  5 0x0000
write  6 0xf0f0
write  7 0xf0f0
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0001
write 17 0x0bff
write 18 0x0fff
write 19 0x0400

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0x020c 0xfa38 0xf9fa 0x0178 0x0542 0x03fe 0xff94 0xf996
0xfb28 0x03cc 0x0650 0x01c8 0xfd1a 0xf9ee 0xfd1e 0x0596
0x0666 0xff3c 0xfb02 0xfb3c 0xff98 0x068e 0x057c 0xfcbc
0xf9a4 0xfd56 0x0232 0x0686 0x03b0 0xfaa8 0xf936 0xffe6
0x0488 0x0578 0x0140 0xf95a 0xf9d4 0x0290 0x063e 0x038a
0xfe8e 0xf908 0xfb68 0x04e8 0x070a 0x00fc 0xfbfc 0xf9c6
0xfdc4 0x0692 0x06c2 0xfe34 0xf9f2 0xfb80 0x0086 0x0744
0x056e 0xfb9c 0xf8c6 0xfdf8 0x034a 0x06e0 0x033c 0xf998

0x01b2 0x07ae 0x07ff 0x07ff 0x07ff 0x01ea 0x0234 0x07ff
0x07ff 0x07ff 0x06dc 0x018a 0x039e 0x07ff 0x07ff 0x07ff
0x0470 0x022e 0x05c8 0x07ff 0x07ff 0x0684 0x0284 0x03bc
0x07ff 0x07ff 0x07ff 0x0412 0x0162 0x0604 0x07ff 0x07ff
0x07ff 0x022a 0x013c 0x07ff 0x07ff 0x07ff 0x07ff 0x011e
0x0224 0x07ff 0x07ff 0x07ff 0x05cc 0x0116 0x03fa 0x07ff
0x07ff 0x07ff 0x0352 0x0220 0x067c 0x07ff 0x07ff 0x0572
0x017c 0x0418 0x07ff 0x07ff 0x07ff 0x02f4 0x0096 0x06bc

0xfa9e 0xf84e 0xfe85 0x0662 0x0729 0x0001 0xf8d8 0xf99d
0x0176 0x07b0 0x0565 0xfd1e 0xf80a 0xfbc8 0x0436 0x07f7
0x02e6 0xfa9e 0xf84e 0xfe85 0x0662 0x0729 0x0001 0xf8d9
0xf99d 0x0178 0x07b1 0x0564 0xfd1d 0xf80a 0xfbca 0x0436
0x07f7 0x02e5 0xfa9d 0xf84f 0xfe87 0x0660 0x072a 0x0002
0xf8d8 0xf99d 0x0176 0x07b0 0x0563 0xfd1e 0xf80a 0xfbc8
0x0436 0x07f7 0x02e5 0xfa9d 0xf84e 0xfe85 0x065f 0x072a
0x0001 0xf8d8 0xf99d 0x0176 0x07b0 0x0565 0xfd1d 0xf80a

0x05ea 0xfdd1 0xf824 0xfb2e 0x038f 0x07ff 0x0392 0xfb31
0xf823 0xfdcd 0x05e7 0x0776 0x00be 0xf935 0xf933 0x00ba
0x0774 0x05ea 0xfdd1 0xf824 0xfb2e 0x038f 0x07ff 0x0394
0xfb31 0xf824 0xfdce 0x05e8 0x0775 0x00be 0xf933 0xf933
0x00bb 0x0775 0x05e9 0xfdd3 0xf824 0xfb2d 0x038e 0x07ff
0x0392 0xfb31 0xf823 0xfdcd 0x05e9 0x0776 0x00bd 0xf935
0xf933 0x00bb 0x0775 0x05e9 0xfdd1 0xf824 0xfb2c 0x038e
0x07ff 0x0392 0xfb2f 0xf823 0xfdcd 0x05e7 0x0775 0x00be
```


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```
# GC3021A diagnostic test D
#
# use the odd parity map, see testA

# control register settings:
write  0 0x0082
write  1 0x8b6e
write  2 0x5bff
write  3 0x0000
write  4 0x00ff
write  5 0x0000
write  6 0x0f0f
write  7 0x0f0f
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0400
write 17 0x0001
write 18 0x0c00
write 19 0x0fff

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0xfec2 0xfe98 0xfb91 0xf901 0xf9bb 0xfcf6 0xff26 0xfddf
0xfa86 0xf8c9 0xfa96 0xfdf4 0xff2f 0xfce8 0xf99e 0xf8f1
0xfba3 0xfebf 0xfed8 0xfbcd 0xf8f7 0xf976 0xfcc3 0xff3d
0xfe27 0xfaaf 0xf8a6 0xfa4d 0xfdd7 0xff5d 0xfd2f 0xf9af
0xf8b9 0xfb60 0xfebb 0xff16 0xfc0a 0xf8ed 0xf933 0xfc91
0xff54 0xfe6e 0xfad7 0xf883 0xfa05 0xfdba 0xff8b 0xfd74
0xf9c0 0xf882 0xfb1e 0xfeb9 0xff56 0xfc44 0xf8e2 0xf8ee
0xfc5d 0xff6b 0xfeb6 0xfaff 0xf860 0xf9be 0xfd9d 0xffba

0xfe7c 0x01c8 0x0321 0x0107 0xfdc7 0xfcf6 0xff7e 0x0296
0x02d7 0xfff5 0xfd1b 0xfd6d 0x0096 0x031d 0x0237 0xfedc
0xfcbf 0xfe35 0x01a5 0x0349 0x014e 0xfdde 0xfcc3 0xff3a
0x028d 0x0313 0x0033 0xfd17 0xfd2a 0x005e 0x032d 0x027c
0xff0c 0xfca2 0xfdec 0x0183 0x0372 0x0194 0xfdf4 0xfc90
0xfef5 0x0283 0x034e 0x0072 0xfd14 0xfce9 0x0026 0x033e
0x02c3 0xff3a 0xfc85 0xfda4 0x0160 0x039b 0x01db 0xfe0b
0xfc5d 0xfeb1 0x0278 0x0389 0x00b1 0xfd10 0xfca6 0xfff0

0x0564 0x07b1 0x0176 0xf99e 0xf8d8 0x0001 0x072a 0x0660
0xfe85 0xf84f 0xfa9e 0x02e6 0x07f7 0x0434 0xfbc9 0xf80a
0xfd1e 0x0565 0x07b1 0x0176 0xf99d 0xf8d8 0x0001 0x072a
0x0660 0xfe87 0xf84f 0xfa9d 0x02e5 0x07f7 0x0436 0xfbc9
0xf80a 0xfd1d 0x0564 0x07b0 0x0178 0xf99d 0xf8d9 0x0002
0x0729 0x065f 0xfe85 0xf84f 0xfa9d 0x02e6 0x07f6 0x0434
0xfbc9 0xf80a 0xfd1d 0x0564 0x07b1 0x0176 0xf99d 0xf8d8
0x0001 0x0729 0x0660 0xfe85 0xf84f 0xfa9e 0x02e5 0x07f7

0x05e8 0xfdd0 0xf823 0xfb2e 0x0392 0x07ff 0x038e 0xfb2d
0xf824 0xfdd3 0x05ea 0x0774 0x00bb 0xf933 0xf934 0x00c0
0x0776 0x05e7 0xfdd0 0xf823 0xfb2f 0x0392 0x07ff 0x038e
0xfb2d 0xf824 0xfdd3 0x05e9 0x0775 0x00bb 0xf933 0xf934
0x00bd 0x0775 0x05e8 0xfdcd 0xf824 0xfb31 0x0394 0x07ff
0x038f 0xfb2c 0xf824 0xfdd3 0x05e9 0x0774 0x00bd 0xf933
0xf934 0x00be 0x0775 0x05e8 0xfdce 0xf823 0xfb31 0x0392
0x07ff 0x038f 0xfb2d 0xf824 0xfdd3 0x05ea 0x0775 0x00bb
```


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```
# GC3021A diagnostic test E
#
# This test uses even parity map.
#
for (i=0;i<256;i++) write (base+i) even_parity(i);
#
# where even_parity(i) is 0x9669 if "i" contains an even number of bits
# and is 0x6996 otherwise (base + 0 = 0x9669, base + 1 = 0x6996, etc)

# control registers settings:
write  0 0x7282
write  1 0x8b6e
write  2 0x7fef
write  3 0x0000
write  4 0x007f
write  5 0x0067
write  6 0x5555
write  7 0x1555
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0bff
write 17 0x0bff
write 18 0x0000
write 19 0x0000

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0xfdae 0xfea6 0xff92 0xfe8e 0xfdde 0x00c4 0xff98 0xfebc
0x01a4 0xfeaa 0xfe06 0x00b4 0x0276 0x0258 0x01e0 0xff54
0xfe86 0xff76 0x003e 0x022e 0x01b8 0x0216 0x021e 0x020e
0x0210 0x007c 0x0130 0x01b0 0x01ee 0x01a2 0x011c 0x0070
0xffba 0xff14 0xffba 0x007c 0xfea4 0xff36 0xfeb2 0xfe76
0xff18 0xfe8c 0xfeda 0xff4e 0xfedc 0xff48 0xffdc 0xfeb8
0xff3e 0x00a6 0x00fc 0x0122 0x0020 0xff04 0xff52 0xffc0
0x0028 0xffba 0x0024 0x00e4 0x00e0 0x00d2 0x00d0 0x00c0

0x01b2 0x027e 0x02c6 0x025e 0x01ba 0x0298 0x02a4 0x0250
0x0208 0x0232 0x019a 0x0268 0x0042 0xff50 0xfe7c 0xfdb8
0xfe2e 0xfdc2 0xfdbe 0xff7a 0xfe9c 0xff62 0x0056 0xff82
0x0038 0x01fc 0x01a0 0x0108 0x0036 0x00fe 0x0184 0x01cc
0x01ca 0x0184 0x01ba 0x01a4 0x00fc 0x0172 0x00f2 0x005e
0xfec0 0x006c 0x00ee 0x0146 0x00d4 0x012c 0x0158 0x0050
0xfef6 0xfeee 0xff48 0xffaa 0xfedc 0xff78 0xff2a 0xfefc
0xff00 0xff0e 0xff10 0xffc8 0x0024 0xffc2 0x0018 0xffc8

0x07e6 0x07ab 0x0675 0x07c5 0x07f4 0x03d4 0x0675 0x07ab
0x00d9 0x07c5 0x07f4 0x03d4 0xfafb 0xf8fa 0xf80c 0xfc2c
0xff27 0xfbd5 0xf9c8 0xf92c 0xf80c 0xf8fa 0xfb4a 0xf92c
0xfafb 0x042b 0x013d 0xfe1f 0xfafb 0xfe1f 0x013d 0x042b
0x0675 0x07c5 0x0675 0x03d4 0x07e6 0x07ab 0x07e6 0x06d4
0xfec3 0x0706 0x07f4 0x07ab 0x07e6 0x07c5 0x0638 0x06d4
0xfec3 0xf83b 0xf81a 0xf8fa 0xf9c8 0x0242 0xff27 0xfbd5
0xf98b 0xfc2c 0xf98b 0xf92c 0xfb4a 0xf8fa 0xfafb 0xf8fa

0xfec3 0x0242 0x04b6 0x01e1 0xff27 0x0706 0x04b6 0x0242
0x07f4 0x01e1 0xff27 0x0706 0x0638 0x03d4 0x00d9 0xf8fa
0xf80c 0xf92c 0xfafb 0x042b 0x00d9 0x03d4 0x0675 0x042b
0x0638 0x06d4 0x07e6 0x07c5 0x0638 0x07c5 0x07e6 0x06d4
0x04b6 0x01e1 0x04b6 0x0706 0xfec3 0x0242 0xfec3 0xfbd5
0xf81a 0xfc2c 0xff27 0x0242 0xfec3 0x01e1 0x0505 0xfbd5
0xf81a 0xfe1f 0x013d 0x03d4 0xfafb 0xf855 0xf80c 0xf92c
0xfb4a 0xf8fa 0xfb4a 0x042b 0x0675 0x03d4 0x0638 0x03d4
```


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```
# GC3021A diagnostic test F
#
# This test uses even parity map, see testE

# control registers settings:
write  0 0x3e02
write  1 0x8b6e
write  2 0x7fef
write  3 0x0000
write  4 0x00ff
write  5 0x00e3
write  6 0x210f
write  7 0x6543
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0aaa
write 17 0x0555
write 18 0x0555
write 19 0x0aaa

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0x07fc 0x07f4 0x07ff 0xfe1e 0xfd96 0xfd94 0xfd14 0xfd12
0x07d0 0x07c8 0xfd0c 0x07ff 0xfd84 0x07ff 0x07ff 0x07ff
0xffb0 0x07ff 0xff12 0xff0e 0x07ff 0x07ff 0x07ff 0x07ff
0x07ff 0x039a 0x07ff 0x07ff 0x07ff 0x07ff 0x075a 0x05c0
0x07ff 0x067c 0x07ff 0x07ff 0x07ff 0x0668 0x07ff 0x07ff
0x065a 0x04cc 0x0408 0x0294 0x01de 0x0088 0x07ff 0x0126
0x07ff 0x0078 0xffda 0x07ff 0x07ff 0x01b6 0x010c 0x07ff
0x0060 0x005a 0x07ff 0x07ff 0x019a 0x0194 0x07ff 0x07ff

0x05d6 0x05d4 0x05ea 0xfff4 0xff4c 0xff44 0xfe96 0xfe8e
0x05c4 0x05c0 0xfe80 0x05d6 0xff1e 0x05e4 0x05ea 0x05d4
0x0178 0x05e2 0x00dc 0x00d4 0x05de 0x05ba 0x059a 0x053e
0x0502 0x0414 0x04bc 0x0418 0x03b4 0x02da 0x0562 0x04ec
0x03bc 0x0524 0x0358 0x035a 0x02ea 0x0518 0x035e 0x0362
0x0510 0x0484 0x042c 0x0368 0x02f4 0x01f8 0x058e 0x026e
0x056c 0x01e6 0x015c 0x058a 0x056a 0x02cc 0x0250 0x0588
0x01c6 0x01c0 0x0588 0x0542 0x02ae 0x02aa 0x0542 0x0542

0xfd5b 0xf8b6 0xf87d 0xfccf 0xf8a2 0xfd2c 0xf8cb 0xfd8b
0xfd5b 0xf8b6 0xf8cb 0xf88f 0xf8a2 0xf86c 0xf841 0xf822
0xfbef 0xf835 0xf841 0xfc1b 0xf82b 0xf812 0xf804 0xf801
0xf809 0xf9fa 0xf815 0xf82f 0xf856 0xf886 0xf8f9 0xf946
0xf856 0xf912 0xf8f9 0xf864 0xf8cb 0xf912 0xf8f9 0xf864
0xf92b 0xf97e 0xf9da 0xfa3e 0xfaab 0xfb1f 0xf804 0xfad1
0xfaab 0xfb1f 0xf81a 0xf808 0xf801 0xfa86 0xfaf8 0xf808
0xf80c 0xfb1f 0xf804 0xf801 0xf801 0xfa86 0xfa62 0xf801

0x078c 0x034a 0x02be 0x0755 0x031c 0x077a 0x0377 0x079c
0x078c 0x034a 0x0377 0x02ed 0x031c 0x028f 0x01ff 0x016b
0x06e3 0x01ce 0x01ff 0x06fc 0x019d 0x0108 0x0072 0xffdb
0xff45 0x0543 0xfee1 0xfe4d 0xfdbb 0xfd2c 0x03d1 0x0452
0xfdbb 0x03fd 0x03d1 0xfd8b 0x0377 0x03fd 0x03d1 0xfd8b
0x0428 0x04a5 0x051d 0x058d 0x05f5 0x0656 0x0072 0x0616
0x05f5 0x0656 0x013a 0x00a4 0x000e 0x05d3 0x0637 0x00a4
0x00d6 0x0656 0x0072 0xffdb 0x000e 0x05d3 0x05b1 0xffdb
```


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```
# GC3021A diagnostic test G
#
# This test uses even parity map, see testE

# control registers settings:
write  0 0x0002
write  1 0x8b6e
write  2 0x7bff
write  3 0x0000
write  4 0x003f
write  5 0x0000
write  6 0xffff
write  7 0x3210
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0555
write 17 0x0aaa
write 18 0x0aaa
write 19 0x0555

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0xf800 0xfe57 0xfafb 0xf800 0x0195 0xf800 0x00cb 0xf800
0xf978 0xff96 0xf800 0x0221 0xf800 0xfcb6 0xfcb4 0xf800
0x021e 0xf800 0xff92 0xf978 0xf800 0x00c3 0xf800 0x018a
0xf800 0xfafa 0xfe50 0xf800 0x0243 0xf800 0xfe1b 0xfb36
0xf800 0x019e 0xf800 0x0099 0xf805 0xf941 0xffb6 0xf800
0x0204 0xf800 0xfc78 0xfce8 0xf800 0x021a 0xf800 0xff5b
0xf9b4 0xf800 0x00d9 0xf800 0x0164 0xf800 0xfac3 0xfe7c
0xf800 0x0235 0xf800 0xfde3 0xfb6d 0xf800 0x01a9 0xf800

0x0178 0x07ff 0xfda9 0x07ff 0x020a 0x0492 0x07ff 0xfe3c
0x07ff 0xff7a 0x07cc 0x06f3 0x0015 0x07ff 0xfdf9 0x07ff
0x03b5 0x02dd 0x07ff 0xfdcb 0x07ff 0x00c4 0x0617 0x07ff
0xfefb 0x07ff 0xfea8 0x07ff 0x0572 0x014e 0x07ff 0xfdc1
0x07ff 0x0249 0x0458 0x07ff 0xfe38 0x07ff 0xffad 0x078f
0x0729 0xfff7 0x07ff 0xfe18 0x07ff 0x03f2 0x02ac 0x07ff
0xfdd3 0x07ff 0x00fc 0x05db 0x07ff 0xfee7 0x07ff 0xfecf
0x07ff 0x05aa 0x0124 0x07ff 0xfdd0 0x07ff 0x0280 0x0422

0xf8ca 0x07f5 0xf999 0x02fd 0x014a 0xfacf 0x0798 0xf835
0x05bd 0xfdfb 0xfdb8 0x05ed 0xf827 0x0781 0xfb04 0x0105
0x033d 0xf971 0x07fb 0xf8e8 0x0425 0xffff 0xfbdd 0x0717
0xf805 0x068f 0xfcc2 0xfefd 0x04fb 0xf880 0x07d9 0xfa13
0x024a 0x0205 0xfa44 0x07ca 0xf868 0x0533 0xfeb4 0xfd04
0x0666 0xf80b 0x0736 0xfb9e 0x0047 0x03e7 0xf90c 0x07fe
0xf948 0x037e 0x00bd 0xfb3e 0x0767 0xf81a 0x061d 0xfd73
0xfe42 0x0589 0xf846 0x07ad 0xfa98 0x0191 0x02b8 0xf9c7

0xfc8b 0xff36 0x04cc 0xf896 0x07e5 0xf9eb 0x0283 0x01cb
0xfa6f 0x07bd 0xf856 0x055f 0xfe7b 0xfd3c 0x0640 0xf812
0x0750 0xfb6e 0x0083 0x03b3 0xf929 0x07ff 0xf929 0x03b4
0x0082 0xfb6e 0x074f 0xf812 0x0641 0xfd3b 0xfe7c 0x055e
0xf856 0x07bd 0xfa6e 0x01cc 0x0281 0xf9ed 0x07e3 0xf895
0x04cd 0xff36 0xfc8d 0x06b0 0xf802 0x06fb 0xfc0d 0xffc5
0x0456 0xf8cf 0x07f6 0xf992 0x0308 0x013e 0xfad9 0x0794
0xf832 0x05c5 0xfdef 0xfdc4 0x05e4 0xf829 0x0785 0xfafc
```


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```
# GC3021A diagnostic test H
#
# This test uses even parity map, see testE

# control registers settings:
write  0 0x0002
write  1 0x8b6e
write  2 0x7bff
write  3 0x0000
write  4 0x00ff
write  5 0x0000
write  6 0x8888
write  7 0xcdef
write  8 0x1fff
write  9 0x1fff
write 10 0x1fff
write 11 0x1fff
write 12 0xff22

write 16 0x0fff
write 17 0x0fff
write 18 0x0001
write 19 0x0001

# perform snapshot
write 12 0xff22
write 12 0xff26
# wait until bit 3 (0x0008) of register 12 goes high

# the snapshot should be:
0x0408 0xfd30 0x00c4 0x0186 0xfc9f 0x0446 0xfc12 0x0272
0xffc3 0xfdf1 0x03c5 0xfb99 0x03c2 0xfdfc 0xffad 0x0296
0xfbe3 0x0476 0xfc7d 0x0189 0x00e6 0xfce9 0x0467 0xfb8e
0x0332 0xfeff 0xfe83 0x0391 0xfb61 0x0459 0xfd32 0x006f
0x0213 0xfc00 0x04c8 0xfbd2 0x025a 0x002b 0xfd5a 0x0463
0xfb25 0x03ec 0xfe29 0xff36 0x0335 0xfb4a 0x04db 0xfc68
0x0146 0x016c 0xfc45 0x04f8 0xfb3b 0x0330 0xff56 0xfdf0
0x0436 0xfada 0x049a 0xfd4a 0x0005 0x02b0 0xfb5c 0x0540

0xfec1 0x032b 0xfbd1 0x03fd 0xfd5e 0x0081 0x01c9 0xfc6b
0x0458 0xfc26 0x023c 0x000a 0xfdad 0x03f3 0xfb90 0x03a5
0xfe38 0xff65 0x02d8 0xfbbc 0x0475 0xfca4 0x0148 0x0131
0xfcab 0x0486 0xfb98 0x0302 0xff46 0xfe38 0x03c9 0xfb4a
0x0446 0xfd69 0x0025 0x025d 0xfbcd 0x04d4 0xfbf1 0x021a
0x0078 0xfd11 0x048e 0xfb21 0x03c4 0xfe6f 0xfee6 0x0379
0xfb27 0x04d3 0xfc9a 0x00fb 0x01be 0xfc05 0x0511 0xfb4d
0x02f5 0xffa7 0xfd9f 0x046f 0xfaca 0x047b 0xfd8d 0xffb1

0x0713 0xf805 0x0694 0xfcbb 0xff04 0x04f4 0xf883 0x07dc
0xfa0c 0x0253 0x01fa 0xfa4b 0x07c8 0xf864 0x053a 0xfea9
0xfd10 0x065e 0xf80c 0x073c 0xfb93 0x0056 0x03da 0xf913
0x07ff 0xf940 0x038c 0x00ad 0xfb4b 0x0760 0xf818 0x0626
0xfd62 0xfe53 0x057c 0xf84b 0x07b2 0xfa8b 0x01a4 0x02a7
0xf9d4 0x07ea 0xf8a4 0x04ae 0xff5c 0xfc6b 0x06c4 0xf801
0x06e8 0xfc2e 0xffa1 0x0475 0xf8c0 0x07f3 0xf9a9 0x02e7
0x0160 0xfabe 0x079e 0xf83a 0x05ad 0xfe10 0xfda4 0x05f9

0xfc45 0xff87 0x048c 0xf8b4 0x07ef 0xf9b8 0x02ce 0x017b
0xfaa9 0x07a7 0xf841 0x059a 0xfe29 0xfd89 0x060d 0xf81e
0x0770 0xfb29 0x00d7 0x0367 0xf957 0x07fd 0xf8fe 0x0400
0x002b 0xfbb5 0x072a 0xf808 0x0676 0xfce9 0xfed2 0x051c
0xf871 0x07d2 0xfa2e 0x0223 0x022c 0xfa28 0x07d3 0xf875
0x0514 0xfedb 0xfce0 0x067d 0xf808 0x0726 0xfbbe 0x0024
0x0407 0xf8fa 0x07fd 0xf95c 0x035f 0x00e1 0xfb22 0x0773
0xf820 0x0606 0xfd92 0xfe20 0x05a2 0xf83f 0x07a4 0xfab0
```


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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
GC3021A-PQ	LIFEBUY	QFP	PCM	160	24	TBD	Call TI	Call TI		CARRIER/MIXER GC3021A-PQ GRAYCHIP	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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